

Diagram illustrating a cross-sectional view of a semiconductor device. The device includes a substrate 100 and a top layer 112. A central region 102 contains a series of rectangular structures 104. A layer 120 is on top of 100, with a patterned layer 122 and a top layer 128. A dashed line 126' indicates a boundary.

FIG. 1A

$$F, G, Z, A$$

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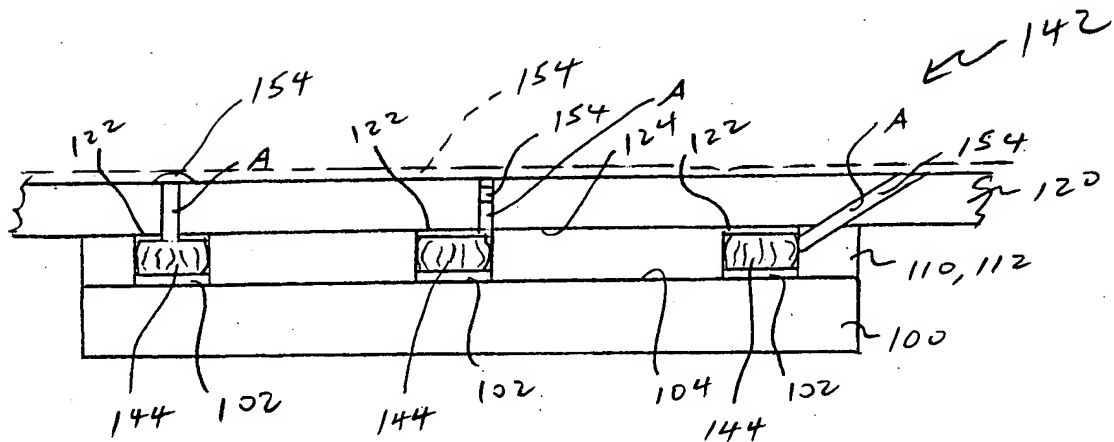


FIG. 3

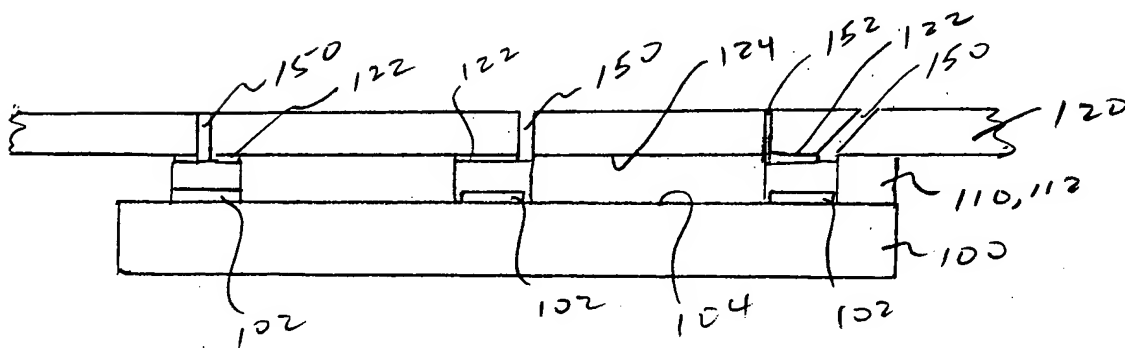


FIG. 4

TITLE: METHODS RELATING TO FORMING INTERCONNECTS
AND RESULTING ASSEMBLIES

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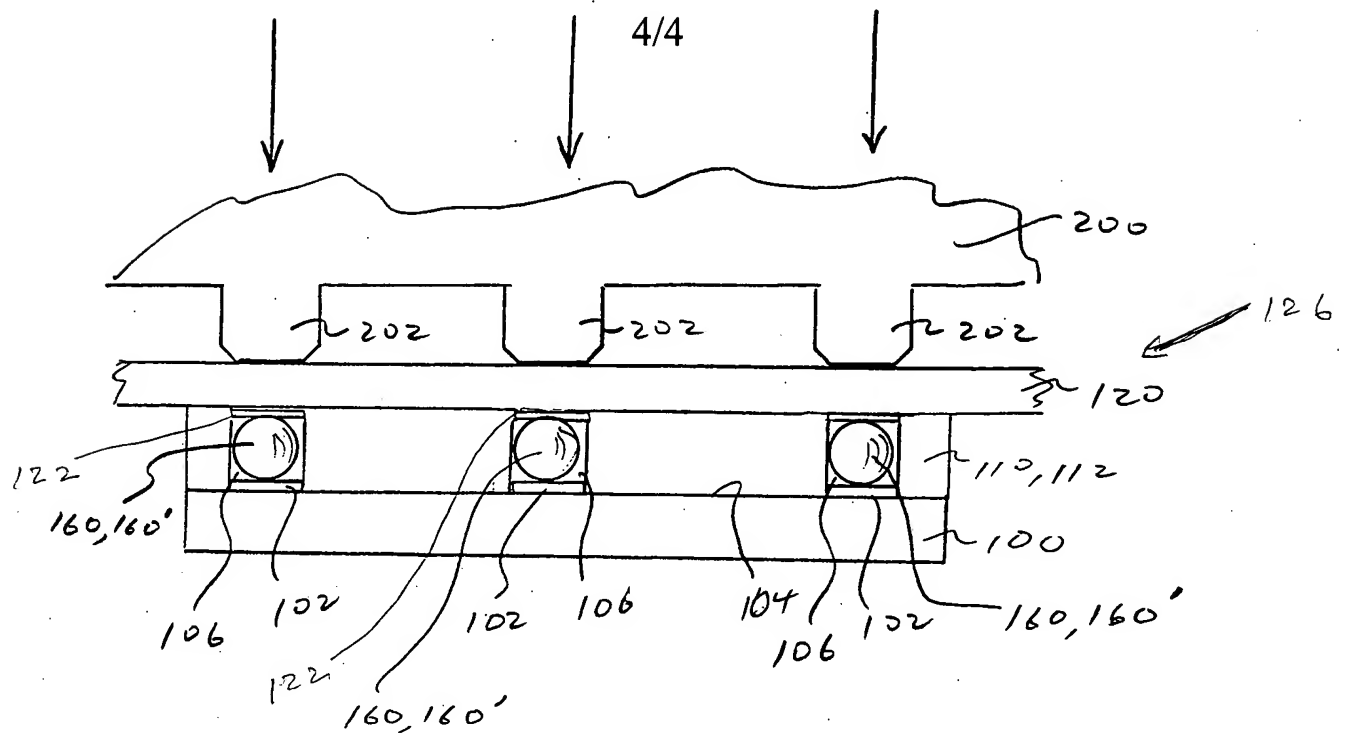


FIG. 5